THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GARY L. SWOBODA and MARTIN D. DANIELS

Appeal No. 95-4501
Application 07/827,549[1]

ON BRIEF

Before THOMAS, KRASS, and CARMICHAEL, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

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[1] Application for patent filed January 29, 1992. According to appellants, this application is a continuation of Application 07/387,475, filed July 31, 1989, now abandoned.

This is a decision on appeal from the final rejection of claims 1 through 32, all of the claims pending in the application.

The invention pertains to the improvement of emulation, simulation and testability architecture and methods in data processing devices. More particularly, a data processing device, comprising a processor and on-chip peripheral circuitry, ordinarily operable together, and formed on a single chip, has the capability of selectively entering externally supplied data into the processor and on-chip peripherals circuitry for starting and stopping operations of the processor and the on-chip peripheral circuitry independently of each other in an emulation mode of operation.

Representative independent claim 1 is reproduced as follows:

1. A data processing device formed in a single semiconductor chip comprising:

an electronic processor, and on-chip peripheral circuitry ordinarily operative together; and

means for selectively entering externally supplied data into the electronic processor and on-chip peripheral circuitry and starting and stopping operations of the electronic processor and the on-chip peripheral circuitry independently of each other in an emulation mode of operation.

The examiner relies on the following references:

Hester et al. (Hester)	4,788,683	Nov. 29, 1988
Daniels et al. (Daniels)	4,860,290 (filed Jun. 2, 1987)	Aug. 22, 1989

Claims 1 through 32 stand rejected under 35 U.S.C. 102(e) or 103, in the alternative, as anticipated by, or unpatentable over, Daniels. Additionally, claims 17 and 18 stand rejected under 35 U.S.C. 103 as unpatentable over Hester in view of Daniels.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

We reverse.

Each of the independent claims 1, 11, 17, 21 and 23 calls for, in one form or another, starting and/or *stopping* operations of a processor and on-chip peripheral circuitry *independently* of each other. Claim 11 specifically requires the execution of different stops *selectively determined by the contents of said mode register*.

The examiner's only substantive explanation of where to find such limitations in Daniels occurs at pages 10-11 of the answer, in responding to appellants' argument that there is no such teaching in Daniels. The examiner states:

> ...one of ordinary skill in the DP art would clearly see the ability to isolate and test the circuits independently. Daniels [sic, Daniels'] teaching of control of the timing module...seems a clear teaching...of something capable of starting and stopping operations. From Daniels' teaching of a CPU which can execute instructions...one...would readily conclude that halt/stop instructions might be executed.

The initial burden is on the examiner to make out a prima facie case of anticipation and/or obviousness with regard to the claimed subject matter. Although the examiner has pointed to various, broad sections of the Daniels disclosure (column 4, lines 30 through 63, column 8, line 57 through column 9, line 50, column 19, lines 19 through 23), the examiner never specifically points out the particular part or parts of the Daniels disclosure which anticipate or make obvious the claimed starting and/or stopping operations. As appellants state, at page 5 of the principal brief, appellants are left "to speculate as to how [the] examiner concludes that the

limitations...are either taught or made obvious by the cited portions of the Daniels text."

Especially in light of appellants' contention that Daniels fails to teach or suggest the claimed feature of "starting and stopping operations...," the examiner had the burden to specifically point out exactly where, in Daniels, these limitations were taught or suggested. Failure to do so constitutes a failure to establish a prima facie case of anticipation and/or obviousness.

Although the examiner states that the skilled artisan, having Daniels before him/her "would clearly see the ability to isolate and test the circuits independently," this does not identify what portion of Daniels teaches or suggests the claimed "starting and stopping." Although the examiner contends that the timing circuit of Daniels is "a clear teaching...of something capable of starting and stopping operations," this, too, does not identify a teaching or suggestion of the claimed "starting and stopping..." The examiner does not identify what this "something" capable of being started and stopped, comprises. Further, the examiner's identification of a "CPU which can execute instructions" in

Daniels does not present a teaching or suggestion of the claimed limitation of "starting and stopping" and the examiner's reasoning that one could "conclude that halt/stop instructions *might* be executed" [emphasis ours] also does not persuade us of any teaching or suggestion in Daniels of "starting and stopping operations of the electronic processor and the on-chip peripheral circuitry independently of each other," as claimed. That something *might* be done falls far short of a suggestion to do it.

We also note that while appellants' arguments are not very compelling, basically merely denying that Daniels teaches or suggests the claimed limitations, and, had the examiner established a prima facie case for anticipation and/or obviousness, appellants' arguments would not appear to carry much weight, the fact remains that the initial burden for establishing such a prima facie case rests with the examiner and the examiner, here, has simply failed to establish such.

Appellants admit that "the module in Daniels are selectively excludable from the scan path in order to provide the capability of realizing shorter scan paths and faster testing times when desired" [reply brief-page 2]. While it

may very well be that such exclusion of a module from a scan path might be considered a “stopping” operation of peripheral circuitry, as broadly claimed, this was not part of the examiner’s rejection or rationale therefor and we will not speculate at this point in the prosecution as to whether or not an exclusion of a module is tantamount to stopping operation of that module, or peripheral circuit.

It is the examiner’s job to establish an anticipation through a specific correlation of claimed elements to elements in the prior art and/or to establish obviousness through a convincing line of reasoning based on teachings and/or suggestions from the prior art. Unless and until the examiner has done so, appellants are under no obligation to present specific arguments distinguishing the claimed invention from the applied prior art for to do so would amount to speculation on appellants’ part as to the exact nature of the examiner’s rejection. Thus, while we find, in the instant case, that appellants’ arguments comprise substantially nothing more than a general denial that Daniels (and for claims 17 and 18, a combination of Hester and Daniels) teaches or suggests the claimed “starting and stopping operations...,” no more was

required in the face of the examiner's failure to specifically set forth a prima facie case of anticipation and/or obviousness, specifically identifying where, and how, Daniels, and/or Hester and Daniels in the case of the additional rejection of claims 17 and 18, suggests the claimed limitation of "starting and stopping operations..."

We make no representations that the instant claimed subject matter may not somehow be anticipated, or made obvious, by Daniels and/or Hester. We reverse the instant rejections solely on the grounds that the examiner has failed to present any convincing line of reasoning that would establish a prima facie case of anticipation and/or obviousness.

The examiner's decision rejecting claims 1 through 32 under 35 U.S.C. 102(e)/103 over Daniels and claims 17 and 18 under 35 U.S.C. 103 over Hester in view of Daniels is reversed.

REVERSED

James D. Thomas Administrative Patent Judge	)
Errol A. Krass Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
James T. Carmichael Administrative Patent Judge	)

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